

8-bit high-speed analog-to-digital converter**TDA8714****FEATURES**

- 8-bit resolution
- Sampling rate up to 75 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.7 effective bits at 4.43 MHz full-scale input at $f_{clk} = 75$ MHz)
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage regulator
- Power dissipation only 340 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

- High-speed analog-to-digital conversion for:
- video data digitizing
 - radar pulse analysis
 - transient signal analysis
 - high energy physics research
 - $\Sigma\Delta$ modulators
 - medical imaging.

GENERAL DESCRIPTION

The TDA8714 is an 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 75 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	25	27	mA
I_{CCD}	digital supply current		-	27	30	mA
I_{CCO}	output stages supply current		-	16	18	mA
I_{ILE}	DC integral linear error		-	± 0.4	± 0.5	LSB
DLE	DC differential linearity error		-	± 0.2	± 0.35	LSB
$AILE$	AC integral linearity error	note 1	-	± 0.5	± 1.0	LSB
$f_{clk(max)}$	maximum clock frequency TDA8714/7 TDA8714/6 TDA8714/4		75 60 40	- -	-	MHz MHz MHz
P_{tot}	total power dissipation		-	340	400	mW

Note

1. Full-scale sine wave ($f_i = 4.43$ MHz; $f_{clk} = 75$ MHz).

7110826 0077179 T&T

8-bit high-speed analog-to-digital converter

TDA8714

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				SAMPLING FREQUENCY
	PINS	PIN POSITION	MATERIAL	CODE	
TDA8714T/4	24	SO24L	plastic	SOT137-1	40 MHz
TDA8714M/4	24	SSOP24M	plastic	SOT340-1	40 MHz
TDA8714T/6	24	SO24L	plastic	SOT137-1	60 MHz
TDA8714M/6	24	SSOP24M	plastic	SOT340-1	60 MHz
TDA8714T/7	24	SO24L	plastic	SOT137-1	75 MHz
TDA8714M/7	24	SSOP24M	plastic	SOT340-1	75 MHz

BLOCK DIAGRAM

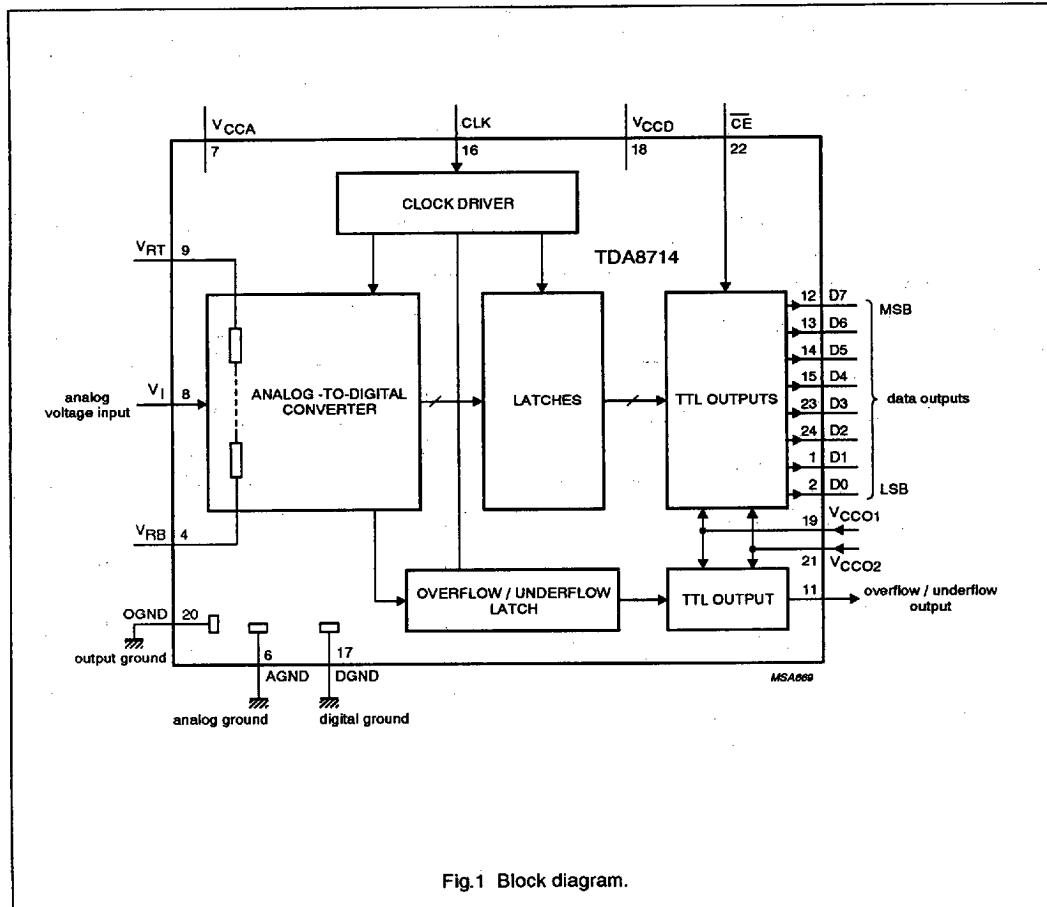


Fig.1 Block diagram.

7110826 0077180 7T1

8-bit high-speed analog-to-digital converter

TDA8714

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output; bit 1
D0	2	data output; bit 0 (LSB)
n.c.	3	not connected
V _{RB}	4	reference voltage BOTTOM input
n.c.	5	not connected
AGND	6	analog ground
V _{CCA}	7	analog supply voltage (+5 V)
V _I	8	analog input voltage
V _{RT}	9	reference voltage TOP input
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output; bit 7 (MSB)
D6	13	data output; bit 6
D5	14	data output; bit 5
D4	15	data output; bit 4
CLK	16	clock input
DGND	17	digital ground
V _{CCD}	18	digital supply voltage (+5 V)
V _{CCO1}	19	supply voltage for output stages 1 (+5 V)
OGND	20	output ground
V _{CCO2}	21	supply voltage for output stages 2 (+5 V)
CE	22	chip enable input (TTL level input, active LOW)
D3	23	data output; bit 3
D2	24	data output; bit 2

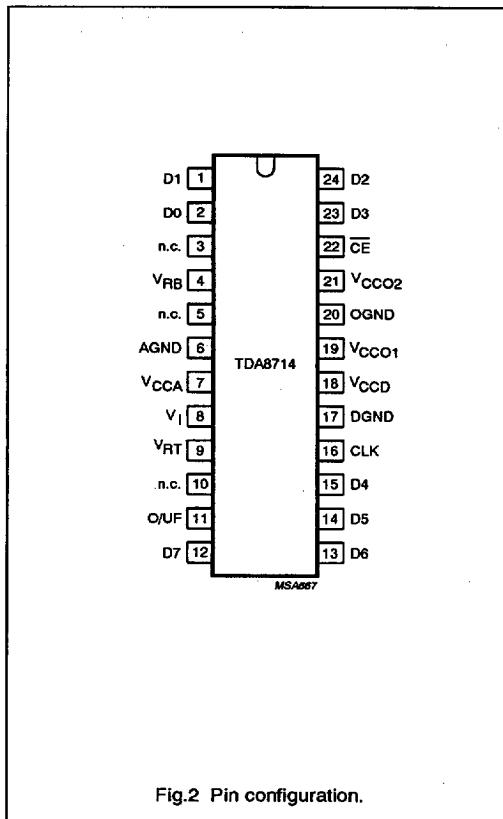


Fig.2 Pin configuration.

8-bit high-speed analog-to-digital converter

TDA8714

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CCA}	analog supply voltage	note 1	-0.3	+7.0	V
V _{CCD}	digital supply voltage	note 1	-0.3	+7.0	V
V _{CCO}	output stages supply voltage	note 1	-0.3	+7.0	V
ΔV _{CC}	supply voltage differences between V _{CCA} and V _{CCD}		-1.0	+1.0	V
ΔV _{CC}	supply voltage differences between V _{CCO} and V _{CCD}		-1.0	+1.0	V
ΔV _{CC}	supply voltage differences between V _{CCA} and V _{CCO}		-1.0	+1.0	V
V _I	input voltage	referenced to AGND	-0.3	+7.0	V
V _{clk(p-p)}	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	V _{CCD}	V
I _O	output current		-	10	mA
T _{stg}	storage temperature		-55	+150	°C
T _{amb}	operating ambient temperature		0	+70	°C
T _j	junction temperature		-	+150	°C

Note

1. The supply voltages V_{CCA} and V_{CCD} may have any value between -0.3 V and +7.0 V provided the difference between V_{CCA} and V_{CCD} is between -1 V and +1 V.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air SOT137-1 SOT340-1	75 119	K/W K/W

8-bit high-speed analog-to-digital converter

TDA8714

CHARACTERISTICS

$V_{CCA} = V_7 \text{ to } V_6 = 4.75 \text{ to } 5.25 \text{ V}$; $V_{CCD} = V_{18} \text{ to } V_{17} = 4.75 \text{ to } 5.25 \text{ V}$; $V_{CCO} = V_{19} \text{ and } V_{21} \text{ to } V_{20} = 4.75 \text{ to } 5.25 \text{ V}$; AGND and DGND shorted together; $V_{CCA} \text{ to } V_{CCD} = -0.25 \text{ to } +0.25 \text{ V}$; $V_{CCO} \text{ to } V_{CCD} = -0.25 \text{ to } +0.25 \text{ V}$; $V_{CCA} \text{ to } V_{CCO} = -0.25 \text{ to } +0.25 \text{ V}$; $T_{amb} = 0 \text{ to } +70^\circ\text{C}$; typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5 \text{ V}$ and $T_{amb} = 25^\circ\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	25	27	mA
I_{CCD}	digital supply current		-	27	30	mA
I_{CCO}	output stages supply current		-	16	18	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); NOTE 1						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.4 \text{ V}$	-400	-	-	μA
I_{IH}	HIGH level input current	$V_{clk} = 2.7 \text{ V}$	-	-	300	μA
Z_i	input impedance	$f_{clk} = 75 \text{ MHz}$	-	2	-	$\text{k}\Omega$
C_i	input capacitance	$f_{clk} = 75 \text{ MHz}$	-	4.5	-	pF
INPUT CE (REFERENCED TO DGND) SEE TABLE 2						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	-	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4 \text{ V}$	-400	-	-	μA
I_{IH}	HIGH level input current	$V_{IH} = 2.7 \text{ V}$	-	-	20	μA
V _i (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW level input current	$V_i = 1.2 \text{ V}$	-	0	-	μA
I_{IH}	HIGH level input current	$V_i = 3.5 \text{ V}$	60	130	180	μA
Z_i	input impedance	$f_i = 4.43 \text{ MHz}$	-	10	-	$\text{k}\Omega$
C_i	input capacitance	$f_i = 4.43 \text{ MHz}$	-	14	-	pF
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.2	1.3	1.6	V
V_{RT}	reference voltage TOP		3.5	3.6	3.9	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.9	2.3	2.7	V
I_{ref}	reference current		-	11.5	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		-	0.24	-	Ω/K
V_{osB}	offset voltage BOTTOM	note 2	-	255	-	mV
V_{osT}	offset voltage TOP	note 2	-	300	-	mV

8-bit high-speed analog-to-digital converter

TDA8714

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
DIGITAL OUTPUTS D7 TO D0 (REFERENCED TO DGND)						
V _{OL}	LOW level output voltage	I _O = 1 mA	0	-	0.4	V
V _{OH}	HIGH level output voltage	I _O = -0.4 mA	2.7	-	V _{CCD}	V
		I _O = -1 mA	2.4	-	V _{CCD}	V
I _{OZ}	output current in 3-state mode	0.4 V < V _O < V _{CCD}	-20	-	+20	μA
Switching characteristics						
CLOCK INPUT CLK (NOTE 1; SEE FIG.3)						
f _{clk(max)}	maximum clock frequency TDA8714/4 TDA8714/6 TDA8714/7		40	-	-	MHz
			60	-	-	MHz
			75	-	-	MHz
t _{CPH}	clock pulse width HIGH		6	-	-	ns
t _{CPL}	clock pulse width LOW		6	-	-	ns
Analog signal processing						
LINEARITY						
ILE	DC integral linearity error		-	±0.4	±0.5	LSB
DLE	DC differential linearity error		-	±0.2	±0.35	LSB
AILE	AC integral linearity error	note 3	-	±0.5	±1.0	LSB
BANDWIDTH (f _{clk} = 40 MHz)						
B	-0.5 dB analog bandwidth	full-scale sine wave	-	12	-	MHz
		75% full-scale sine wave	-	18	-	MHz
t _{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave; Fig.12; note 4	-	2.5	3.5	ns
t _{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave; Fig.12; note 4	-	3.0	4.0	ns
HARMONICS (f _{clk} = 40 MHz)						
h ₁	fundamental harmonics (full scale)	f _i = 4.43 MHz	-	-	0	dB
h _{all}	harmonics (full scale); all components second harmonics third harmonics	f _i = 4.43 MHz	-	-64	-60	dB
			-	-58	-55	dB
THD	total harmonic distortion	f _i = 4.43 MHz	-	-56	-	dB
SIGNAL-TO-NOISE RATIO (NOTE 6; SEE FIG.7 AND FIG.13)						
S/N	signal-to-noise ratio (full scale)	without harmonics; f _{clk} = 40 MHz; f _i = 4.43 MHz	46	48	-	dB

7110826 0077184 347

8-bit high-speed analog-to-digital converter

TDA8714

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS (NOTE 6; SEE FIGS.7 AND 13)						
EB	effective bits TDA8714/4	$f_{clk} = 40 \text{ MHz}$ $f_i = 4.43 \text{ MHz}$ $f_i = 7.5 \text{ MHz}$	-	7.75	-	bits
	effective bits TDA8714/6	$f_{clk} = 60 \text{ MHz}$ $f_i = 4.43 \text{ MHz}$ $f_i = 7.5 \text{ MHz}$ $f_i = 10 \text{ MHz}$	-	7.7	-	bits
	effective bits TDA8714/7	$f_{clk} = 75 \text{ MHz}$ $f_i = 4.43 \text{ MHz}$ $f_i = 7.5 \text{ MHz}$ $f_i = 10 \text{ MHz}$ $f_i = 15 \text{ MHz}$	-	7.7	-	bits
TWO-TONE (NOTE 7)						
TTIR	two-tone intermodulation rejection	$f_{clk} = 40 \text{ MHz}$	-	-56	-	dB
BIT ERROR RATE						
BER	bit error rate	$f_{clk} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz};$ $V_i = \pm 16 \text{ LSB at code 128}$	-	10^{-11}	-	times/samples
DIFFERENTIAL GAIN (NOTE 5)						
G _{diff}	differential gain	$f_{clk} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz}$	-	0.6	-	%
DIFFERENTIAL PHASE (NOTE 5)						
Φ _{diff}	differential phase	$f_{clk} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz}$	-	0.8	-	deg
Timing (note 8; see Figs 3 and 5; $f_{clk} = 75 \text{ MHz}$)						
t _{ds}	sampling delay time		-	-	2	ns
t _h	output hold time		5	-	-	ns
t _d	output delay time		-	10	11	ns
3-state output delay times (see Fig.4)						
t _{dZH}	enable HIGH		-	6	10	ns
t _{dZL}	enable LOW		-	12	16	ns
t _{dHZ}	disable HIGH		-	50	54	ns
t _{dLZ}	disable LOW		-	10	14	ns

8-bit high-speed analog-to-digital converter**TDA8714****Notes to the "Characteristics"**

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 00 up to and including FF:
 - a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at $T_{amb} = 25^\circ\text{C}$.
 - b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to FF at $T_{amb} = 25^\circ\text{C}$.
3. Full-scale sine wave ($f_i = 4.43 \text{ MHz}$; $f_{clk} = 75 \text{ MHz}$).
4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
5. Measurement carried out using video analyser VM700A.
6. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: $S/N = EB \times 6.02 + 1.76 \text{ dB}$.
7. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
8. Output data acquisition: the output data is available after the maximum delay time of t_d ; in the event of 75 MHz clock operation, the hardware design must take into account the t_d and t_h limits with respect to the input characteristics of the acquisition circuit.

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8-bit high-speed analog-to-digital converter

TDA8714

Table 1 Output coding and input voltage (typical values; referenced to AGND).

STEP	$V_I(p-p)$	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.555	1	0	0	0	0	0	0	0	0
0	1.555	0	0	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1
.
.
254	.	0	1	1	1	1	1	1	1	0
255	3.30	0	1	1	1	1	1	1	1	1
Overflow	>3.30	1	1	1	1	1	1	1	1	1

Table 2 Mode selection.

CE	D7 TO D0	O/UF
1	high impedance	high impedance
0	active; binary	active

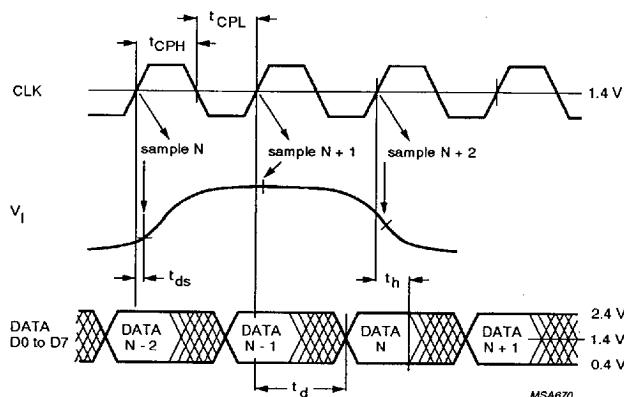
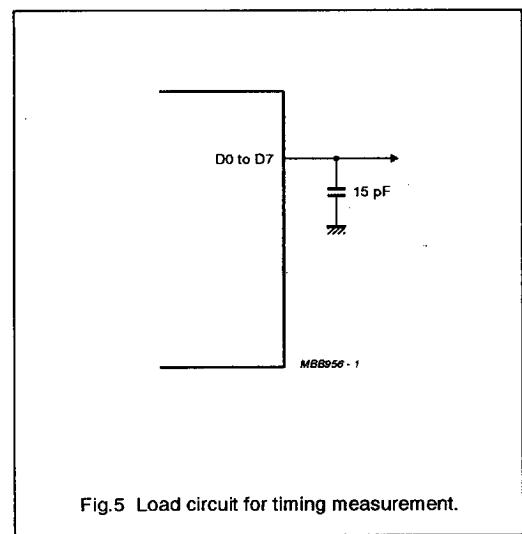
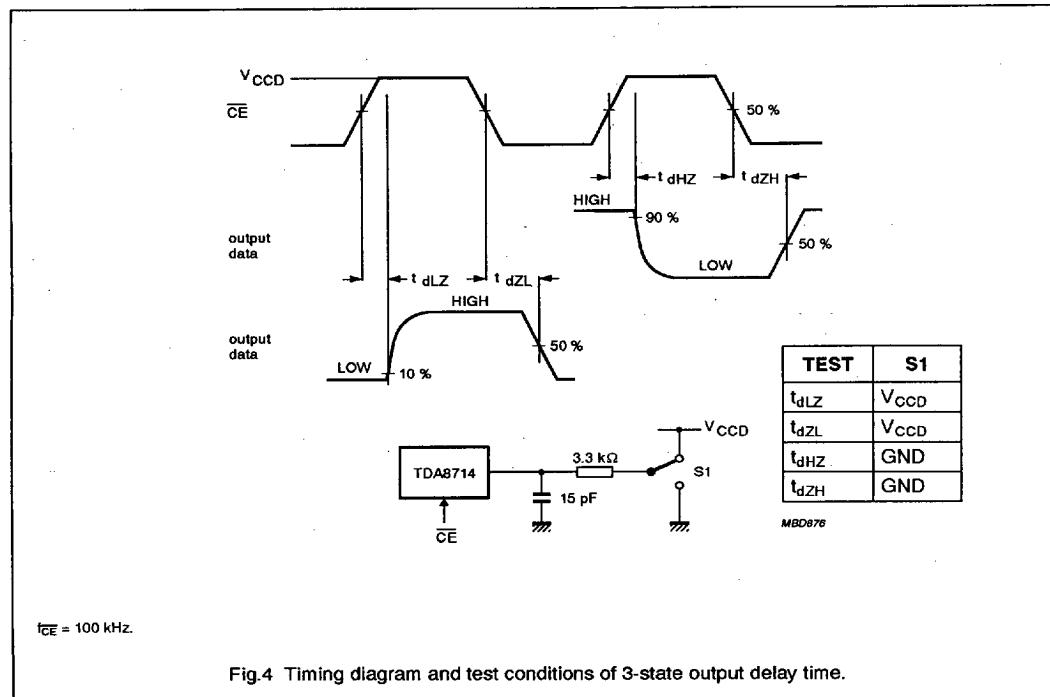


Fig.3 Timing diagram.

8-bit high-speed analog-to-digital converter

TDA8714



8-bit high-speed analog-to-digital converter

TDA8714

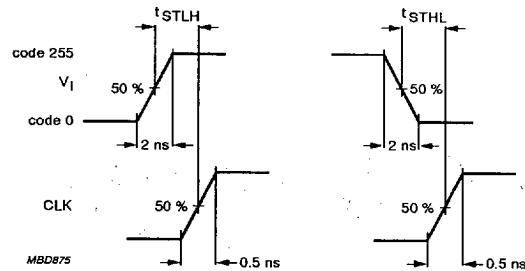
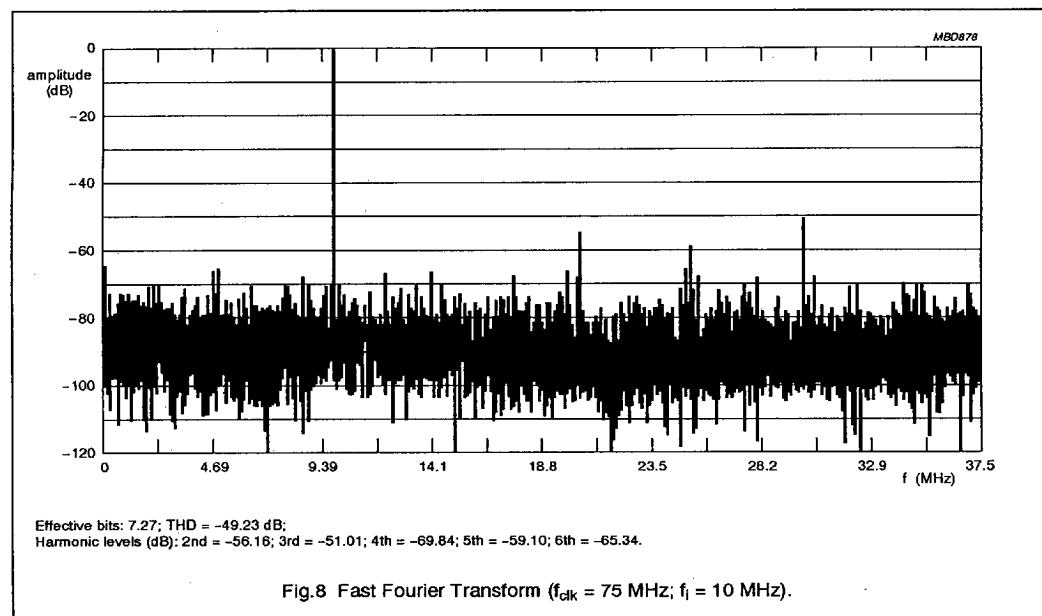
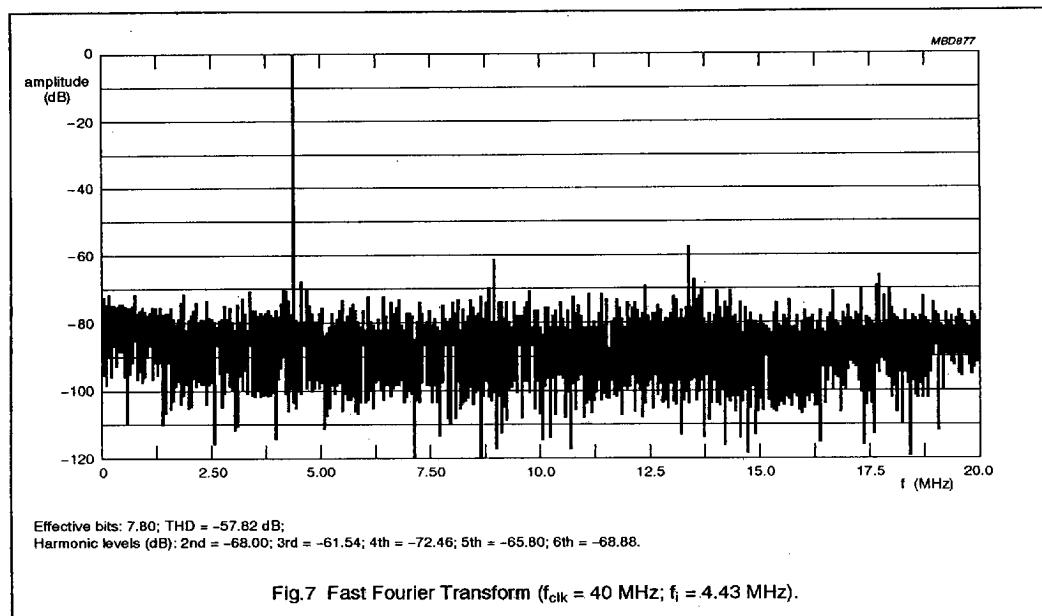


Fig.6 Analog input settling-time diagram.

8-bit high-speed analog-to-digital converter

TDA8714



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TDA8714

INTERNAL PIN CONFIGURATIONS

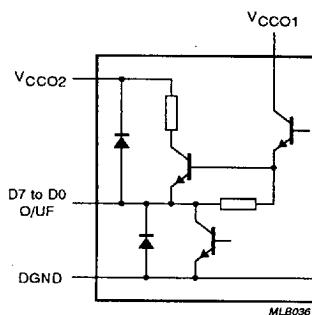


Fig.9 TTL data and overflow/underflow outputs.

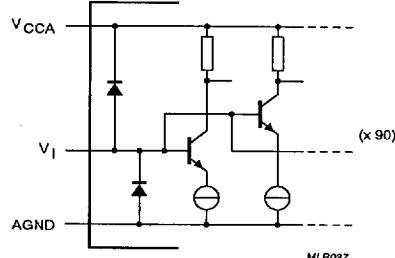
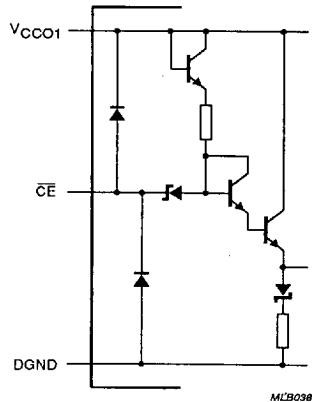
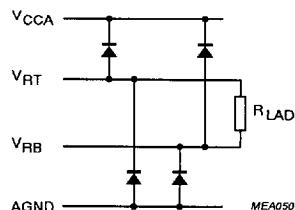


Fig.10 Analog inputs.

Fig.11 \overline{CE} (3-state) input.Fig.12 V_{RB} and V_{RT} .

8-bit high-speed analog-to-digital converter

TDA8714

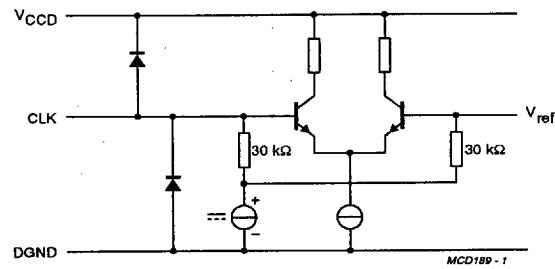
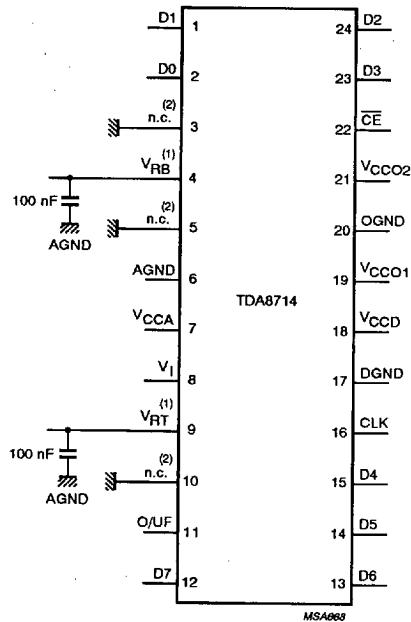


Fig.13 CLK input.

8-bit high-speed analog-to-digital converter

TDA8714

APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value.

(1) V_{RB} and V_{RT} are decoupled to AGND.

(2) Pin 5 should be connected to AGND; pins 3 and 10 to DGND in order to prevent noise influence.

Fig.14 Application diagram.